EECS 645 Project: L1 Cache Simulator

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**Abstract**

The purpose of this project is to programmatically simulate the behavior of an L1 cache. Written and implemented in C, the cache is set at a size of 32 KB, with each block being 64 bytes in size. Because this model is only simulating the behavior of a cache, actual data is not stored. Instead, address traces are read from binary files and used to store tags, meta-data, and determine whether or not a block is valid. Additionally, this project implements a replacement algorithm based upon temporal locality.

Finally, the address traces are used to determine whether or not “hits” are achieved in the cache during simulation. From there, the hit probability is calculated for the cache when using three different access methods: 1) First Index Fastest, 2) Last Index Fastest, and 3) Random Index. The results are displayed as the output once the program has been ran.

**Principles of Operation**